IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

1-13 (Canceled)

14. (Currently Amended) A semiconductor memory device having a memory structure in which a plurality of 5-transistor cells each including first and second CMOS (complementary metal oxide semiconductor) inverter circuits ~~each~~ having a latch structure and a control transistor which is connected between a storage node of the first CMOS inverter circuit and a bit line and whose gate is connected to a word line are connected in parallel to a plurality of bit lines and a plurality of word lines, the semiconductor memory device comprising:

at least one VSS power line connected to a source terminal of an N-type MOS transistor of at least the second CMOS inverter circuit of each of the 5-transistor cells connected to the bit lines; and

at least one selection circuit which applies a second voltage VSS+ΔV, which is higher than a first voltage VSS, to the source terminal of the N-type MOS transistor of the second CMOS inverter circuit of the 5-transistor cells through said at least one VSS power line at least in "1" data write mode.

15. (Original) The semiconductor memory device according to claim 14, wherein the second voltage VSS+ΔV is set at 105% to 130% of the first voltage VSS.

16. (Original) The semiconductor memory device according to claim 14, wherein said at least one VSS power line is connected to a source terminal of an N-type MOS transistor of the first CMOS inverter circuit of each of the 5-transistor cells connected to the bit lines, and said at least one selection circuit applies the second voltage VSS+ΔV to source

terminals of N-type MOS transistors of the first and second CMOS inverter circuits of the 5-transistor cells through said at least one VSS power line at least in the "1" data write mode.